AMENDMENTS TO THE CLAIMS

Claims 1-4 (canceled)

Claim 5 (amended): ~~The signaling device of claim 34, further comprising~~ A signaling device comprising:

a signal generator generating a plurality of output signals at a plurality of respective time intervals, wherein said signal generator further comprises a second plurality of delay cells respectively generating the plurality of output signals;

a plurality of time interval control units regulating the respective time intervals of the plurality of output signals, wherein said plurality of time interval control units individually control the respective time intervals between the plurality of output signals so as to produce substantially uniform time spacing between each of the plurality of output signals, wherein said plurality of time interval control units are a first plurality of delay cells used to delay respective ones of the plurality of output signals based on a plurality of individual control signals respectively received by the first plurality of delay cells;

a plurality of output buffers respectively outputting a plurality of substantially uniformly time spaced channel signals; and

a plurality of delay comparators, wherein each delay comparator receives predetermined ones of the plurality of channel signals output from said plurality of output buffers and produces respective ones of the individual controls signals received by the first plurality of delay cells.

Claim 6 (previously presented): The signaling device of claim 5, further comprising a plurality of charge pump units respectively coupled to said plurality of delay comparators, wherein each charge pump unit converts the individual control signals produced by said plurality of delay comparators into a compatible form used by the first plurality of delay cells.

Claim 7 (amended): ~~The signaling device of claim 3,~~ A signaling device comprising:

a signal generator generating a plurality of output signals at a plurality of respective time intervals, wherein said signal generator further comprises a second plurality of delay cells respectively generating the plurality of output signals;

a plurality of time interval control units regulating the respective time intervals of the plurality of output signals, wherein said plurality of time interval control units individually control the respective time intervals between the plurality of output signals so as to produce substantially uniform time spacing between each of the plurality of output signals, wherein said plurality of time interval control units are a first plurality of delay cells used to delay respective ones of the plurality of output signals based on a plurality of individual control signals respectively received by the first plurality of delay cells;

a plurality of output buffers respectively outputting a plurality of substantially uniformly time spaced channel signals; and

wherein said second plurality of delay cells are in a ring oscillator used in a phase locked loop (PLL):-based multi-phase clock generator system.

Claim 8 (canceled)

Claim 9 (allowed): A time-interleaved architecture comprising:

a first set of delay cells arranged in series, wherein each of said first set of delay cells produces a delayed output signal; and

a second set of delay cells respectively coupled to ones of said first set of delay cells, said second set of delay cells receiving delayed output signals produced by respective ones of said first set of delay cells and respectively outputting channel output signals in response to the received delayed output signals;

wherein each of said second set of delay cells receives a unique control signal controlling the timing of the channel output signal output by each of said second set of delay cells.

Claim 10 (allowed): The time-interleaved architecture as recited in claim 9, wherein a plurality of the unique control signals received by said second set of delay cells are based on unique combinations of the channel output signals output by said second set of delay cells, and wherein the unique control signals individually control the timing of the channel output signals so as to produce substantially uniform time spacing between transitions of the channel output signals.

Claim 11 (allowed): The time-interleaved architecture as recited in claim 10, wherein a designated one of the unique control signals received by said second set of delay cells is aligned to an external reference clock.

Claim 12 (allowed): The time-interleaved architecture as recited in claim 11, wherein the designated one of the unique control signals is output from a feedback loop in response to a designated one of the channel output signals output by one of said second set of delay cells.

Claim 13 (allowed): The time-interleaved architecture as recited in claim 9, wherein each of said first set of delays cells is associated with at least two delay cells of said second set of delay cells.

Claim 14 (allowed): The time-interleaved architecture as recited in claim 9, further comprising a set of output buffers, wherein each of said set of output buffers is respectively coupled to one of the delay cells in said second set of delay cells to buffer the channel output signal output by the one delay cell in said second set of delay cells.

Claim 15 (allowed): The time-interleaved architecture as recited in claim 14, wherein the time-interleaved architecture is within an integrated electronic system permitting real-time calibration of the channel output signals output by said second set of delay cells.

Claim 16 (allowed): A multi-phase clock generator system for generating a plurality of channel output signals for use in a multi-channel application, the multi-phase clock generator comprising:

a phase detector receiving both a reference clock signal and a first channel output signal provided by a first channel of the multi-channel application, said phase detector outputting directional control signals based on a comparison of output phases of the reference clock signal and the first channel output signal so as to align the first channel output signal with the reference clock signal;

a charge pump providing an output in response to the directional control signals generated by said phase detector;

a loop filter providing a filtered main output control signal corresponding to the output provided by said charge pump;

a first plurality of delay cells;

a plurality of output buffers, wherein at least one output buffer is paired with a respective one of said first plurality of delay cells, said plurality of output buffers

respectively providing a plurality of channel output signals, including the first channel output signal;

a second plurality of delay cells, each coupled between one of said first plurality of delay cells and a paired one of said plurality of output buffers, wherein each of said plurality of delay cells receives an individual delay control signal to control delay of the cell in providing an output signal to its associated output buffer; and

a calibration loop, coupled to said second plurality of delay cells, wherein said calibration loop includes a plurality of delay comparators, each delay comparator respectively outputting individual delay control signals for respective ones of said second plurality of delay cells.

Claim 17 (allowed): The multi-phase clock generator as recited in claim 16, wherein the individual delay control signal received by each of said second plurality of delay cells is distinct and independent of each other to allow independent control of the delay of each of said second plurality of delay cells.

Claim 18 (allowed): The multi-phase clock generator as recited in claim 17, wherein said first plurality of delay cells form a ring oscillator.

Claim 19 (allowed): The multi-phase clock generator as recited in claim 18, wherein said first plurality of delay cells form a delay line in a delay locked loop (DLL).

Claim 20 (allowed): The multi-phase clock generator as recited in claim 19, wherein all but a reference one of said first plurality of delay cells receives as its input channel output signals from said plurality of output buffers, wherein the reference one of said first plurality of delay cells receiving as its input the reference clock signal.

Claim 21 (allowed): The multi-phase clock generator as recited in claim 20, wherein each one of said plurality of delay comparators receiving as an input a different combination of the plurality of channel output signals output by said plurality of output buffers so as to provide simultaneous and independent control of the delay of each of said second plurality of delay cells.

Claim 22 (allowed): A method of calibrating a plurality of channel output signals of a multi-phase clock generator having a first plurality of delay cells paired with at least one of a plurality of output buffers, and a second plurality of delay cells respectively receiving output signals from the first plurality of delay cells and outputting the channel output signals to respective ones of the plurality of output buffers, the method comprising the steps of:

phase aligning a first one of the plurality of channel output signals to an external reference clock; and

individually controlling respective ones of the second plurality of delay cells to individually delay output of the channel output signals to respective ones of the plurality of output buffers.

Claim 23 (allowed): The method of calibrating as recited in claim 22, wherein said individually controlling step comprises the step of comparing combinations of channel output signals from the plurality of output buffers to provide each individual control of each of the second plurality of delay cells.

Claim 24 (allowed): The method of calibrating as recited in claim 23, wherein said individually controlling step further comprises the step of comparing unique combinations of channel output signals from the plurality of output buffers to provide distinct voltage control signals for all but one of the second plurality of delay cells.

Claim 25 (allowed): A method of providing a plurality of clock signals, the method comprising the steps of:

producing a series of delayed output signals; and

outputting a series of channel output signals in response to respective ones of the series of delayed output signals; and

individually controlling the output of each of the series of channel output signals to produce precise timing of each channel output signal output in said outputting step.

Claim 26 (allowed): The method of providing a plurality of clock signals as recited in claim 25, wherein said individually controlling step involves individually controlling the output of each of the series of channel output signals to produce a series of uniformly spaced clock signals.

Claim 27 (allowed): The method of providing a plurality of clock signals as recited in claim 25, wherein said individually controlling step aligns at least one of the channel output signals to a reference clock.

Claim 28 (allowed): The method of providing a plurality of clock signals as recited in claim 27, wherein said individually controlling step aligns the at least one of the channel output signals to a reference clock using an output from a feedback loop comparing the at least one channel output signal and the reference clock signal.

Claim 29 (allowed): The method of providing a plurality of clock signals as recited in claim 26, wherein said individually controlling step controls the output of a plurality of the series of channel output signals based on different channel output signals.

Claim 30 (allowed): The method of providing a plurality of clock signals as recited in claim 29, wherein said individually controlling step controls the output of each of the series of channel output signals based on different combinations of channel output signals.